Specialized FPGA and SoC
Design Services

AIP-ST2059

Time Synchronization over Internet Protocol

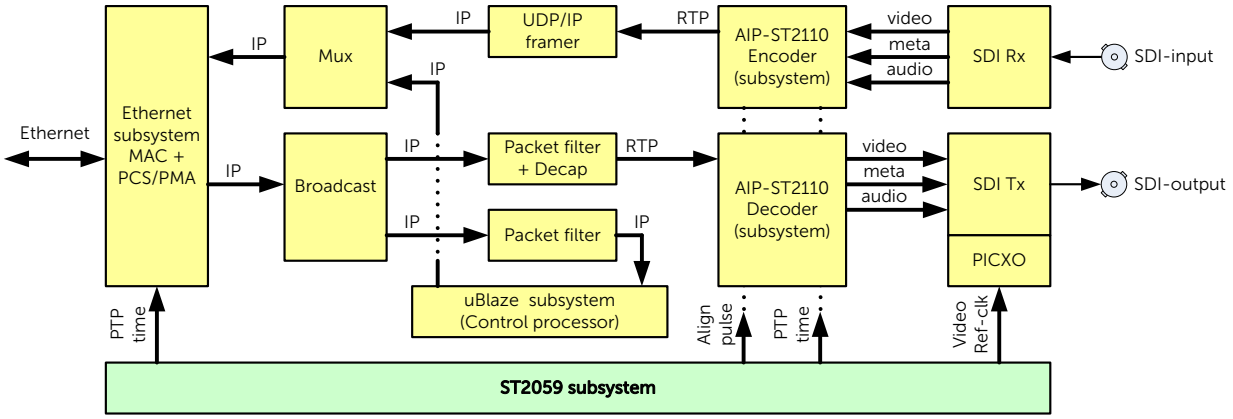

Figure 1: Application example

The AIP-ST2059 is an FPGA IP core that generates timing and clock signals according to the SMPTE ST 2059 standard defined by the Society of Motion Picture and Television Engineers. These deterministic timing signals can be used to time synchronize audio and video systems to a SMPTE ST2059 (PTP) grandmaster.

Product Description

The IP core provides broadcast and professional AV equipment the ability to support deterministic generation of timing (signals) for video and audio systems.
The Adeas AIP-ST2059 core uses the IEEE 1588 Precision Time Protocol (PTP) to generate time-aligned synchronization and reference clock signals, thus permitting the interoperable use of IP-based media equipment.
It supports timing and synchronization according to:

- ST 2059-1: Alignment of Signals to Epoch
- ST 2059-2: Profile for IEEE1588 PTP

Based on standard AXI4-Stream, AXI4-Lite and AXI4-MM interfaces, the AIP-ST2059 core can easily be integrated into your system design. RTL, SW drivers and a ST2059 daemon are included.

Key Features & Benefits

- Fast locking performance
- Generation of HH:MM:SS:FF Time Code, including drop frame
- Generation of multiple programmable output reference clock and sync signals
- Implementation is successfully tested during multiple SMPTE and VSF interoperability testing
- Supports the use of non-PTP aware switches, as well as PTP-aware transparent and boundary clocks
- The AIP-ST2059 core is network speed independent, so can be used in 1G, 10G, 25G and 100G Ethernet networks.

Available demo designs

- Based on Xilinx KC705 and KCU105 development kits
- Supports 1Gb or 10Gb Ethernet networks
- Generates SDI black frame output and DARS (AES3) output synchronised to the grandmaster

Available documentation

- Product guide
- Application note

Available licenses

- Site license
- Multi-site license
- Source code license

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