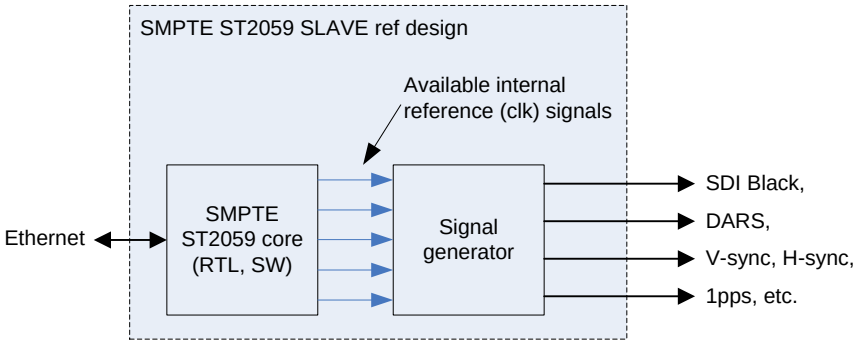
Specialized FPGA and SoC Design Services

AIP-ST2059

Time Synchronization over Internet Protocol



The AIP-ST2059 is an FPGA IP core that generates timing and clock signals according to the SMPTE ST 2059 standard defined by the Society of Motion Picture and Television Engineers. These deterministic timing signals can be used to time synchronize audio and video systems to a SMPTE ST2059 (PTP) grandmaster.

Product Description

The IP core provides broadcast and professional AV equipment the ability to support deterministic generation of timing (signals) for video and audio systems. Audio/visual systems are generally synchronized, locked to the same time base with a relative phase with respect to a master time generator. This makes seamless switching between cameras or mixing a presenter in front of weather graphics possible. The same can be true for audio devices.

The Adeas AIP-ST2059 core uses the IEEE 1588 Precision Time Protocol (PTP) to provide time-aligned signal generation, thus permitting the interoperable use of IP-based media equipment with conventional genlocked SDI equipment.

Based on standard AXI4-Stream, AXI4-Lite and AXI4-MM interfaces, the AIP-ST2059 core can easily be integrated into your system design.

Key Features & Benefits

- Supports timing and synchronization according to SMPTE ST 2059-1 and ST 2059-2.
- Generation of SMPTE ST12-1 Time Code.
- Implementation is successfully tested during interoperability testing.
- The core is network speed independent.

Available reference designs

- Based on Xilinx KC705 and KCU105 development kits.
- Supports 1Gb and 10Gb Ethernet networks.
- Generates SDI black frame output and DARS (AES3) output synchronised to the grandmaster.

Available documentation

- Product guide.
- Application note

Available licenses

- Time limited Evaluation license
- Project license
- Site license
- Worldwide license

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