BROADCAST
SMPTE ST 2059

Adeas

Timing Synchronization through SMPTE ST 2059

Introduction

SMPTE ST 2059 is a standard defining a mechanism for the deterministic generation of timing (signals) for video and audio systems. It is intended to be used to time synchronize related signals. Audio/visual systems have an important requirement in that they must synchronize all signals, locked to the same time base with a relative phase with respect to a master time generator. This makes seamless switching between ` or mixing the weatherman in front of weather graphics possible. A device in this type of system typically has a synchronization input, and an output, for example, a video camera will have a synchronization input and a video output. The camera will align the capturing of the image and the corresponding video output to the synchronization input which is called genlocking. The same can be true for audio devices.

XILINX
ALL PROGRAMMABLE™

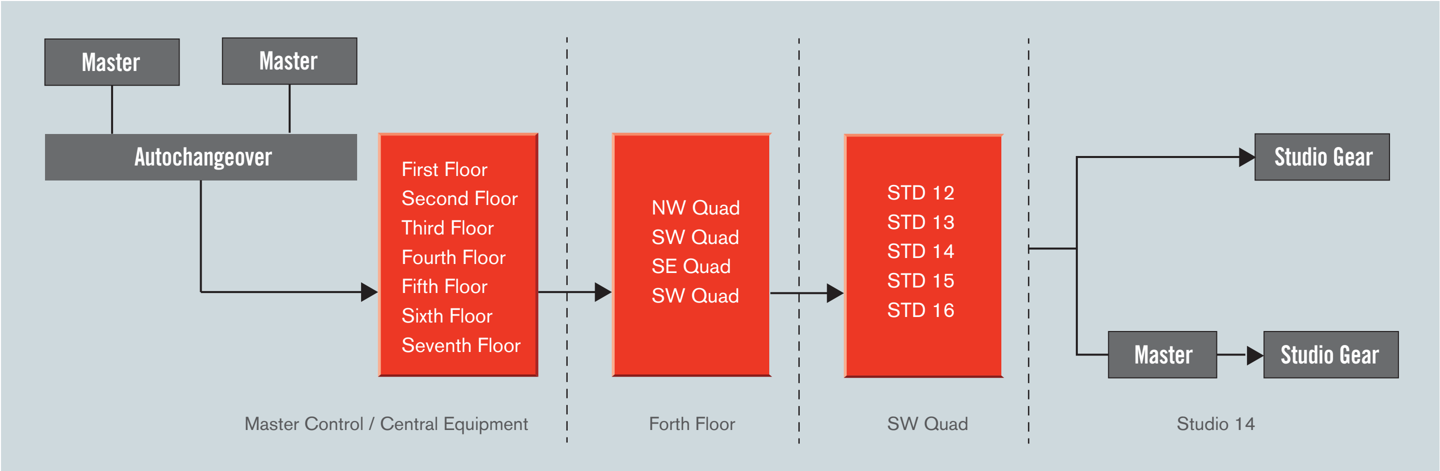

Figure 1 Traditional distribution of synchronization signals in a larger facility

Distribution of the sync signals has not changed much over the last decades. In larger facilities, the synchronization signals are distributed, amplified and routed similarly as shown in Figure 1 above. The video and audio timing is distributed on coax (color black or black burst for video and DARS for audio). Time code signals are mostly distributed on twisted pair. In a TV studio or OB van, multiple cables are needed for audio, video and time code. When a facility has provisions for both 50 Hz and 59.97 Hz frame rates, it must distribute multiple sets of sync signals.

Because some facilities also have provisions for networked data communication (Ethernet), it would be beneficial to use the same network for the distribution of synchronization information. ST 2059 allows for the decentralization of the generation of necessary synchronization signals. The master timing generator only distributes the time, and slaves generate the necessary sync signals locally. Therefore the relationship between time and the various sync signals are defined in ST 2059. Other advantages using ST 2059 are that the same network can be used to transport the audio and video and long distance synchronization is possible using GPS. Also the relationship between audio and video is well defined.

Distributing time on a switched network (Ethernet) with sufficient precision is not a given, as the transportation of data packets from master to slave takes an unknown amount of time. The mechanisms in the IEEE1588 standard, also called Precision Time Protocol (PTP), can take care of distributing precision timing.

ST 2059 is based on IEEE1588 and describes the operating parameters and additional metadata to be used in conjunction to the IEEE1588 precision time protocol, in order to distribute time for the professional broadcast environment.

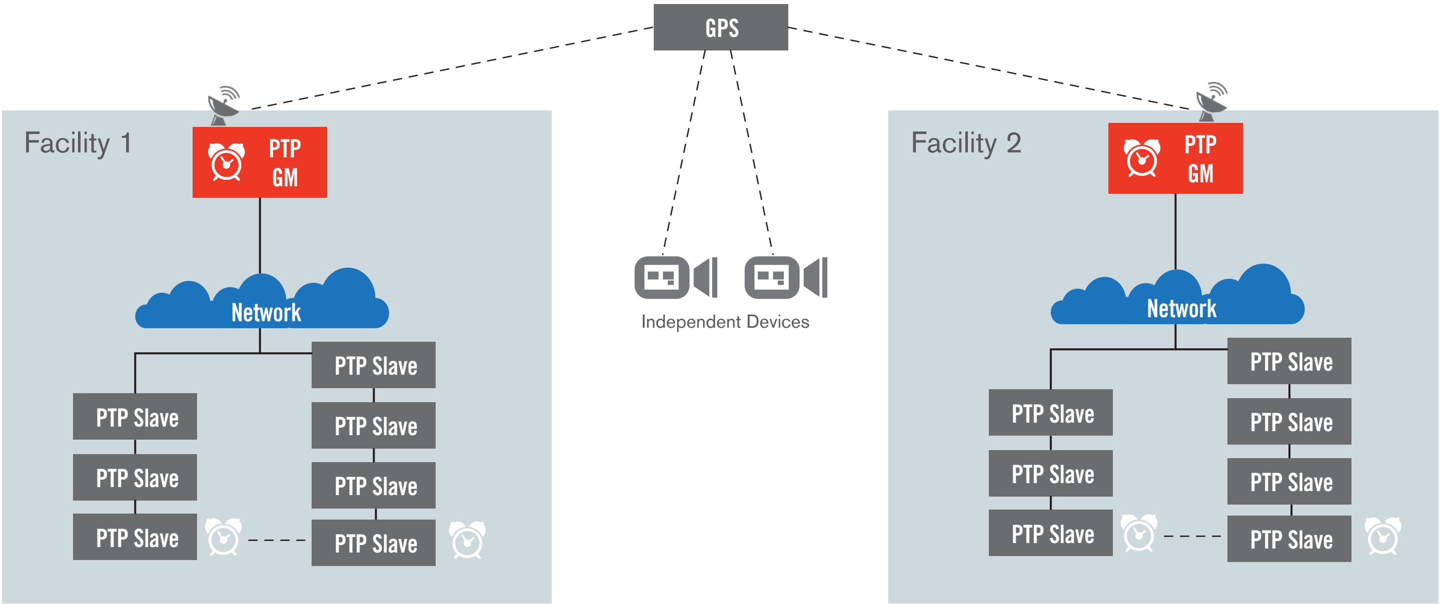

Figure 2 Distribution of synchronization using ST 2059

A grandmaster (GM) timing device is connected via a network to all slave devices, which in turn reproduces the time with regards to the master device so that each slave will have the same time reference. By using this reference, they are able to output their signals with the same time base and same relative phase to each other. Figure 2 demonstrates how the master gets its time from GPS, allowing global synchronization.

USAGE

A solid ST 2059 implementation will completely replace legacy distribution of synchronization. All devices in a facility will have a network connection to the grandmaster, and derive their timing from it. Also the audio and video data can be exchanged using a network.
Examples include:

- **IP Video Camera**
  - An IP camera can be directly connected to an IP network with synchronization input and audio/video output. Other data, such as communication between cameraman and producer, or video return channel can run over the same network.
- **Audio Recording Equipment**
  - Recording audio at multiple locations can be accomplished using the same sample rate and with an exact time relation to a video source.

Currently, there is a large install base of existing equipment (using legacy synchronization inputs). As ST 2059 slowly becomes ubiquitous and embraced by the industry, a move toward a wholesale networked facility will be gradual. Proven synchronization methods, using color black and DARS will be used for some time. There is a strong likelihood that ST 2059 will function in tandem with legacy synchronization methods. Equipment using SMPTE and convertor boxes will fill this need, using local sync generators and devices connecting to the master via Ethernet are needed to output all synchronization signals, such as color black, DARS and time code.

ST 2059-based Synchronization

Each ST 2059 slave reproduces the time base of the Master. The time is in fact an 80 bit digital value and 48 bits represent the amount of seconds elapsed from the Epoch, which is January 1st 1970. The other 32 bits represent the amount of nanoseconds within a second.

Time Reproduced at the Slave

The slave controls its own time base, is able to set it, and is able to increase or decrease its pace. The slave must be able to monitor how much it is off with regards to the master. ST 2059 uses the IEEE1588 mechanisms and has multiple mechanisms

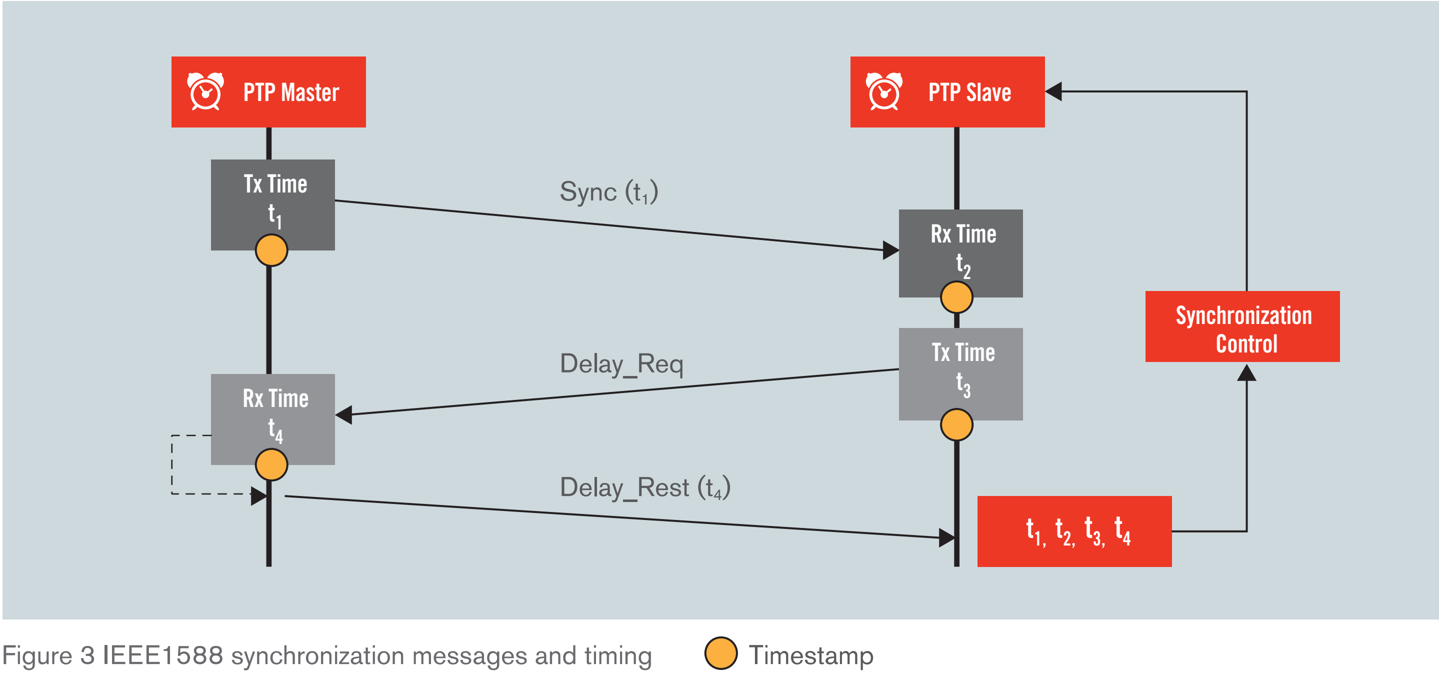

Figure 3 IEEE1588 synchronization messages and timing

to synchronize time, all of them relying on the same principle. One of the mechanisms is the delay request mechanism. The master sends a sync message to the slave containing a timestamp (t1) of the master time (TM), at which the sync message was sent. The slave receives this message and takes a time stamp of the slave time (TS), at the time of reception (t2) of this message. So the slave now knows the difference between the slave and master time plus the network delay from master to slave. (t2 - t1 = network delay MS + TS-TM).

The next step is to determine the network delay from slave to master. A delay request message, containing the timestamp t3, is sent from slave to master. This message arrives at t4 at the master. The master then sends the arrival time (t4) to the slave. From these values the slave can calculate the network delay. (t3-t4 = TS-TM - network delay SM -> network delay SM = TS-TM-t3+t4). Assuming the network delay from master to slave is equal to the network delay of the slave to the master, the formula TS-TM = t2 - t1 – network delay MS = t2 - t1–(TS-TM-t3+t4) can be written. The offset between the master time and the slave time is now known: TS-TM = (t2 - t1 + t3 - t4)/2. This offset is used to control the slave time base in order to minimize the offset. Measurements are performed multiple times per second and the slave can continuously keep track of the master time.

A control loop filter must ensure that the slave time base is initially locked fast enough, and will create the smallest possible offset and timing jitter. ST 2059 specifies 1 micro second of maximum offset within 5 seconds. The IEEE1588 operating parameters that ST 2059 specifies are chosen in a way that is optimized for professional broadcast environments. Examples of parameters are the amount of synchronization messages per second, precision of clocks, transport mechanisms like IPv4 and IPv6.

The Relationship between Time-base and Audio/Video Signals

The ST 2059 standard specifies a relationship that all audio and video signals are signals with a repeating sequence, a video signal is repeatedly transmitting pixels, which form video lines and multiple lines form a video frame and the frames are repeated. ST 2059 specifies the phase of this sequence at a specific instant in the past, called the SMPTE epoch. So for a given video standard (frame rate), the phase of the signal can be calculated at an exact given time.

A DARS audio reference signal is the same. An AES3 signal also has a repeating structure, so for a given audio sample rate, the phase can be calculated at a given time. Having a specified phase of video signals in time and having a specified phase of audio signals in time also means that the relation of audio and video is specified at a certain time.

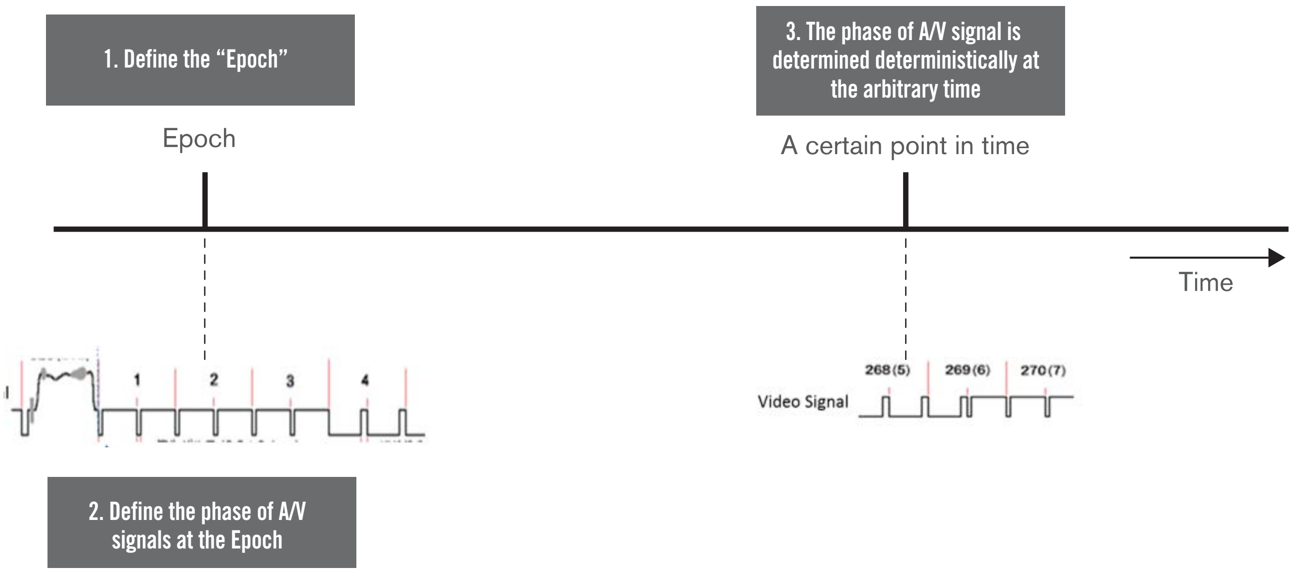

Figure 4 Reference of video signals

Time Code and Leap Seconds

Time code is the current time of day in hours, minutes and seconds combined with the current video frame number. ST 2059 specifies the exact relationship between the time base and the time code. This relationship also incorporates things like leap seconds and daily jam.

A leap second compensates for the mismatch between the UTC (atomic) time and the mean solar time. The International Earth Rotation and Reference Systems Service (IERS) normally decides when leap seconds are applicable.

Counting frame numbers within seconds is not a problem at frame rates that have an exact amount of frames within a second, such as 30Hz. At non-exact frame rates, such as 29.97 Hz, counting frame numbers becomes more difficult. In these cases, the drop frame method together with a daily jam is used. Drop frame in time code does not actually drop frames, but it drops frame numbers in the time code. So instead of counting 28, 29, 00, 01, 02, sometimes the 1st and 2nd frame count is omitted, so counting is: 28, 29, 02, 03, and so on. This is executed once every minute except every 10th minutes. This leaves a remaining error, which is eliminated by a 'daily jam'. A daily jam is the event where a discontinuity is intentionally inserted into the time code sequence in order to remove the accumulated discrepancy between time code and the actual time.

At NAB 2015, Xilinx and Adeas will show a ST 2059 time synchronization implementation combined with a SMPTE 2022-5/6 implementation that is capable of time synchronizing (2) ST 2059 slaves over Ethernet. Each slave is implemented on a KC705 board having a Kintex®-7 FPGA. They are locked to an IEEE1588 / ST 2059 grand master via a gigabit Ethernet network. Each slave is outputting an SDI-black video signal. One is used to lock a video source. The video source is outputting its signal to a SMPTE2022-5/6 converter, also implemented in the Kintex-7, which sends the video over a 10G Ethernet network to the other slave, which converts it back to an SDI signal. An SDI analyzer demonstrates the two slaves are synchronized. A laptop is used as a user interface to control the demo.

About Xilinx in Broadcast and Pro A/V

Xilinx is the worldwide leader of All Programmable FPGAs, SoCs and 3D ICs for the broadcast and pro a/v markets with solutions ranging from video, audio and network connectivity; real-time 8K, 4K and high definition video processing; and video over IP solutions. These solutions enable any media over any network, accelerate time to market and achieve greater innovation and differentiation in broadcast and pro a/v systems. For more information, please visit www.xilinx.com/applications/broadcast.html.

About Xilinx

Xilinx is the world's leading provider of All Programmable FPGAs, SoCs and 3D ICs. These industry-leading devices are coupled with a next-generation design environment and IP to serve a broad range of customer needs, from programmable logic to programmable systems integration. For more information, visit www.xilinx.com.

About ADEAS

Adeas is an independent design house developing customer specific electronics. Adeas is specialized in FPGA & SoC based design services and has extensive experience developing products, boards, modules and IP for market leaders in the broadcast and professional AV industry. Though no products are available under Adeas brand, Adeas (co-)development is present in camera's, modulators, converters, codecs, routers and PCI(E) products for many successful brands today. Adeas boasts more than 100 man years of a programmable logic experience and is a certified Xilinx Alliance Program Member.

Contact Information

Antoine Hermans, CTO
antoine.hermans@adeas.nl
www.adeas.nl

Adeas B.V.
Luchthavenweg 53, 5657EA
Eindhoven, The Netherlands

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India

Meenakshi Tech Park
Block A, B, C, 8th & 13th floors,
Meenakshi Tech Park, Survey No. 39
Gachibowli(V), Seri Lingampally (M),
Hyderabad -500 084
Tel: +91-40-6721-4000
www.xilinx.com

XILINX
ALL PROGRAMMABLE™

Printed in the U.S.A. PN 2460 WW042015