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AIP-FrameBuffer

Video frame Synchronizer for adapting video timing

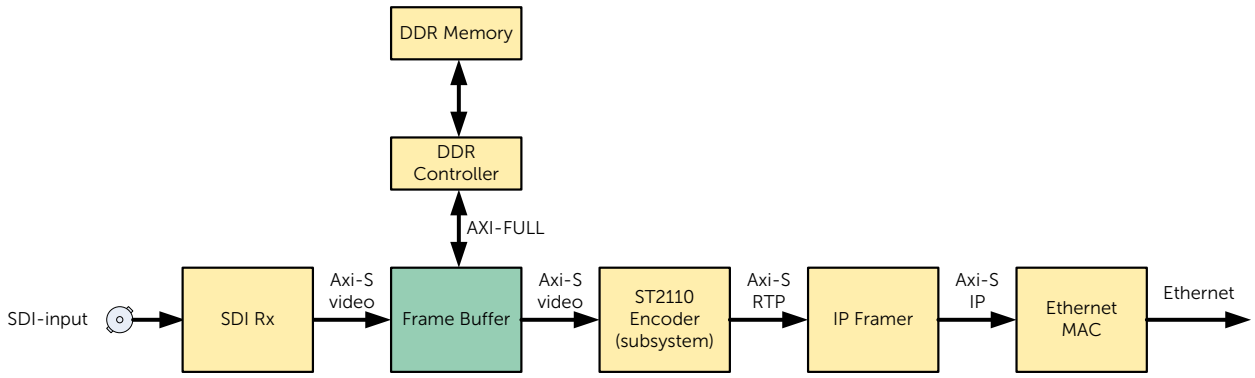

Figure 1: Frame Buffer in an example environment

The AIP-FrameBuffer is an FPGA IP core that buffers one or more video frames. It can be used for adapting the timing (frequency and / or phase) of a video stream, for instance to lock to a house genlock or PTP timing. It also enables uninterrupted video output in case of interrupted or incomplete video input.

Product Description

The Frame Buffer IP core provides broadcast and professional AV equipment makers with the ability to adapt the timing (frame rate and phase offset) of video streams. It can operate in 'full frame drop-and-repeat' mode or in a low-latency mode.
The frame timing can be imposed by the video sink, or by providing a frame-sync signal.

Based on standard AXI4-Stream, AXI4-FULL and AXI4-Lite interfaces, the Frame Buffer can easily be integrated into a video processing system. The RTL core is controlled by a software driver, which is included.

Key Features & Benefits

- Supports 2 or 4 pixels per clock
- Supports 8, 10, 12 or 16 bits per component
- Supports RGB, 4:2:0, 4:2:2, 4:4:4 color schemes
- Supports Interlace, progressive scan and PSF
- Supports resolutions up to 8K and above
- Frame rate 'independent', limited by FPGA clock frequency and memory bandwidth
- 'Drop-and-repeat' mode, or 'Frame tearing' mode for low latency.
- Configurable to allow for easy system customization and resource optimization

Available demo designs

- The Frame Buffer is integrated as part of the Adeas ST 2110 demo designs
- Based on Xilinx development kits

Available documentation

- Product guide

Available licenses

- Site license
- Multi-site license
- Source code license

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