Specialized FPGA and SoC
Design Services

AIP-IPFilter

IP packet filtering and distribution for IPv4

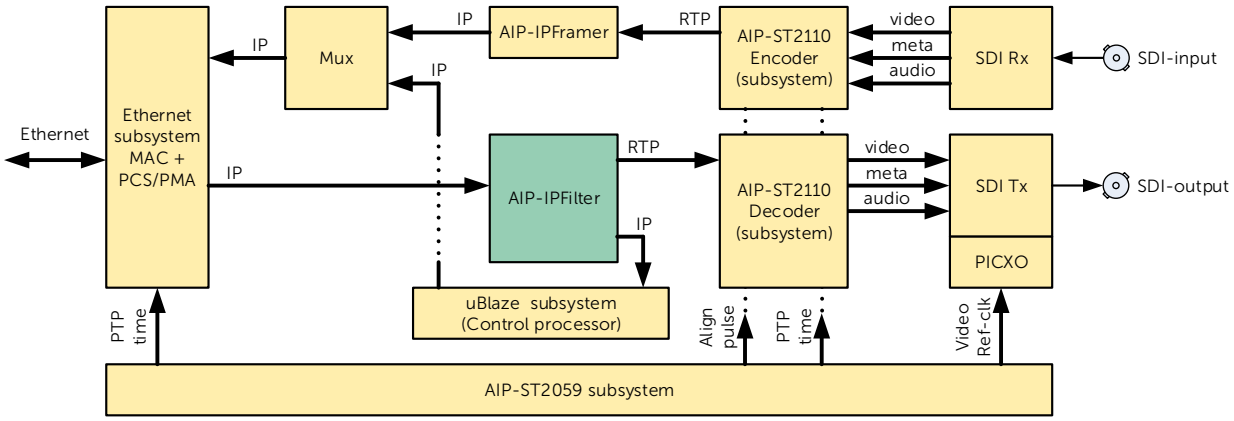

Figure 1: Application example

The AIP-IPFilter is an FPGA IP core that performs filtering and distribution of IP packets in a multi-channel system. It is optimized but not limited to be used in a professional video over IP environment, e.g. in combination with the professional media over IP standard SMPTE-ST2110 and timing standard SMPTE-ST2059.

Product Description

The IP core filters incoming packets from an Ethernet MAC and distributes them to the appropriate channel. Decision making is programmable by SW control, based on IP address or port number.
It removes faulty packets and strips IP, Vlan and/or UDP headers on the media channels. Specific multicast port packet filtering is possible to unload the control processor.

The core is designed to be able to keep up with a fully loaded 100G Ethernet network.

Based on standard AXI4-Stream and AXI4-Lite interfaces, the AIP-IPFilter core can easily be integrated into your system design. RTL and SW drivers are included.

Key Features & Benefits

- Up to 100G Ethernet performance
- Supports IPv4. (IPv6 is optional)
- Supports Vlan headers
- High performance for small and large packets up to an MTU of 1500

Available Demo designs

- The core is used in combined SMPTE-ST2059 and SMPTE-ST2110 demo designs

Available documentation

- Product guide

Available licenses

- Site license
- Multi-site license
- Source code license

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