Specialized FPGA and SoC
Design Services

AIP-SDI BRIDGE

Embedding of media into SDI data streams

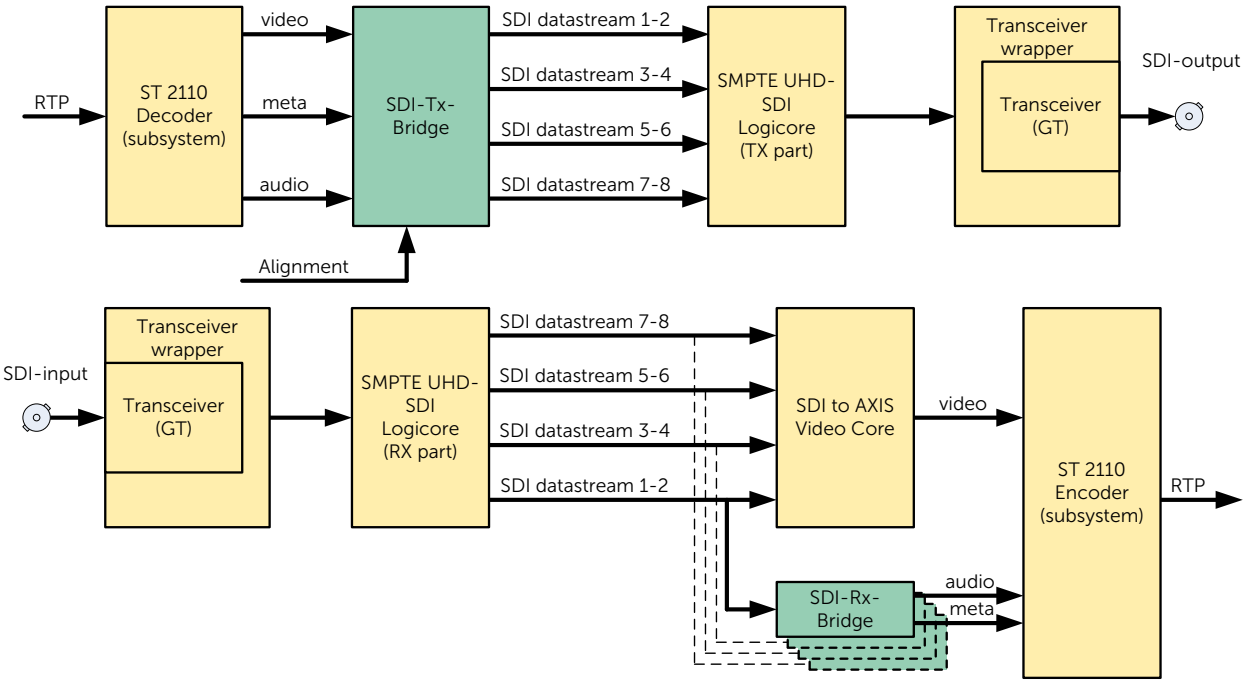

Figure 1: SDI Tx and Rx bridge in an example environment

The AIP-SDI Bridge is an FPGA IP core set consisting of an SDI Tx Bridge and an SDI Rx Bridge which act as companions to the Xilinx UHD SDI Logicore to provide missing functionality. The SDI Tx Bridge provides embedding of audio and ancillary data along with formatting the SDI data stream per SMPTE standards. The SDI Rx Bridge provides de-embedding of audio and ancillary data from an SDI stream. These IP cores are production ready and suitable for use in professional SDI equipment.

Product Description

The IP cores provide broadcast and professional AV equipment with the ability to send and/or receive SDI streams. The timing of the outgoing SDI streams can be synchronized to an (ST 2059) alignment point.

Based on standard AXI4-Stream and AXI4-Lite interfaces, the SDI bridges can easily be integrated into an SDI system. The RTL cores are controlled by a software driver, which is included.

Key Features & Benefits

- Modular and configurable to allow for easy system customization and resource optimization
- Supports HD-SDI, 3G-SDI, 6G-SDI and 12G-SDI
- Precise control of output timing

Available demo designs

- The SDI bridges are integrated as part of the Adeas ST 2110 demo designs
- Based on Xilinx development kits

Available documentation

- Product guide

Available licenses

- Site license
- Multi-site license
- Source code license

Adeas bv, Luchthavenweg 53, 5657 EA Eindhoven
Tel.: +31 (0)40 235 0060, info@adeas.nl, www.adeas.nl