Specialized FPGA and SoC
Design Services

AIP-RTPFailSafe

Seamless protection switching at RTP level

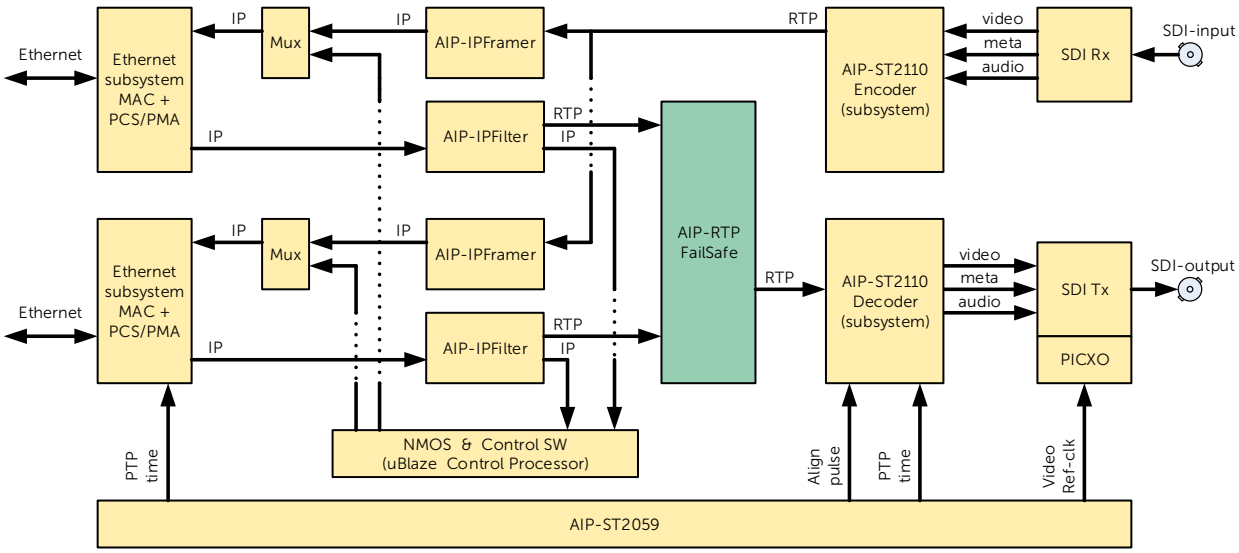

Figure 1: Application example

The AIP-RTPFailSafe is an FPGA IP core that enables the creation of a single reconstructed output stream from 2 redundant input streams through seamless protection switching at RTP datagram level. It is typically used in professional media over IP networks, having a main and a redundant network. Seamless protection is often referenced as SMPTE ST2022-7.

Product Description

The IP core provides broadcast and professional AV equipment Seamless protection switching (hitless failover) using 2 (Ethernet) ports. One RTP stream is reconstructed out of 2 input RTP streams. Buffering of RTP packets is done to be able to cope with Ethernet jitter, latency differences between streams and re-ordered packets.
Based on standard AXI4-Stream, AXI4-Lite and AXI4-MM interfaces, the AIP-RTPFailSafe core can easily be integrated into your system design. The RTL core is controlled by SW driver, which is included.

Key Features & Benefits

- Number of channels configurable up to 16
- External (e.g. DDR4) or internal (BRAM or URAM) can be used for buffering
- Per channel configurable buffer depth, to allow the user to define which ST2022-7 receiver classification to support.
- The AIP-RTPFailSafe core is network speed independent, so can be used in 1G, 10G, 25G and 100G Ethernet networks

Available demo design

- Based on Xilinx development kits
- Supports 10 and 25 Gb/s Ethernet network connections
- Including ST2059 time synchronisation and NMOS control
- Control SW running on a MicroBlaze softcore processor on Peta Linux OS

Available documentation

- Product guide

Available licenses

- Site license
- Multi-site license
- Source code license

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